REMARKS

Claims 1-24 are pending in the application.

Claims 1-5, 11-15 and 21-24 have been rejected.

Claims 6-10 and 16-20 have been objected to.

Claims 1, 2, 5-8, 11, 12, 15-18, 21, and 24 have been amended as set forth herein.

Claims 1-24 remain pending in this application.

Reconsideration of the claims is respectfully requested.

CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 1-5 and 21-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication Patent No. 2004/0114587 to *Huang, et al.* (hereinafter "Huang") in view of "Survey and Taxonomy of IP Address Lookup Algorithms" to *Ruiz-Sanchez, et al.* (hereinafter "Ruiz-Sanchez"). The Applicants respectfully traverse the rejection.

Claims 11-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of Ruiz-Sanchez and further in view of U.S. Patent No. 6,496,510 to *Tsukakoshi, et al,* (hereinafter "Tsukakoshi"). The Applicants respectfully traverse the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re*

Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), *viz.*, (1) the scope and content of the prior art; (2) the differences between the prior art and the claims

at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

Applicants respectfully submit that the cited references do not teach or suggest all the claim limitations of amended Claim 1. Specifically, Claim 1 has been amended to recite, "at least one consecutive identical symbols table associated with said first stage of said trie tree search table."

The Office Action appears to suggest that the skip count mentioned in Paragraphs [0049] to [0051] of Huang refer to consecutive symbols. However, Huang relates to embedding common prefix bits (the "path compression patterns") of a data packet and the length of the pattern (the "skip count") in a parent entry to save memory space that is occupied by single entry trie tables. This embedding also saves the memory bandwidth and power associated with the memory space. Paragraphs [0079] to [0086] of Huang, for example, state:

> [0079] For further explanation and clarification of the operation of the present invention, consider the following example. An exemplary data structure comprises the following set of prefixes, represented as grouped in an equal stride length of four.

P0:	0011 1101 0010 1*	(1)
P1:	0001 0100 0000 1001 0010 1101 001*	(2)
P2:	0001 0100 0000 1001 0010 1101 0110 01*	(3)
P3:	0001 0100 0000 1001 0010 1101 00*	(4)
P4:	0001 0100 0000 1001 0010 1101 1*	(5)
P5:	0001 0100 0000 1001 0010 1101 000*	(6)

[0080] The bitmap that encodes a four (4) bit stride consists of sixteen (16) bits (two (2) to the power of four (4)). The data structure that represents the prefixes P0 through P5 is set forth in FIG. 7. In FIG. 7 the label Tn (where n is a number) denotes a table in pipeline stage n. The label En (where n is a number) denotes an entry in a table. For example, T0 represents the first level trie table (pipeline 1). T1 represents the second level trie table (pipeline 2). T1E1 and T1E2 represent data entry 0 and data entry 1 of table T1. T1E0 represents the T1 table header.

[0081] While each entry in a table may hold many fields, for purposes of explanation and clarity only two fields are shown in the entries shown in FIG. 7. The first is a bitmap field that indicates the number and positions of data entries in the next level or "child" table. The second is a pointer that holds the base address of the next level or "child" table.

[0082] Examining the data structure shown in FIG. 7, one sees two chains of non-leaf single entry trie tables. Table T2a is the only table in the first chain. Tables T2b, T3b, T4b, T5b and T6b form the second chain. Using the optimized path compression process of the invention it is possible to eliminate table T2 by modifying the T1E1 bitmap format. The T1E1 bitmap is replaced with the bit patterns "1101 0010" and its meaning is redefined by creating a type of format that indicates "path compression with one stride." During the search process the lookup logic will interpret the entry as a path compression entry that holds pattern "1101 0010" and handle the entry accordingly.

[0083] Similarly, the optimized path compression process of the invention can be applied to the second chain of non-leaf single entry tables to eliminate the tables. In this case there are five (5) consecutive non-leaf single entry tables that represent six (6) strides of four (4) bit patterns. Because there are only sixteen (16) bits in the bitmap data field, only four (4) strides of patterns can be placed in one entry. The optimized path compression can be achieved by using two consecutive path compression tables. The first table hold four (4) strides of pattern (i.e., 0100 0000 1001 0010) and the second table holds the remaining two (2) strides (1101 0110). The result of applying these steps of the optimized path compression process is shown in FIG. 8.

[0084] The benefits of applying the optimized path compression process of the invention are quite apparent in this case. There are ten (10) tables in the original data structure shown in FIG. 7. These ten (10) tables contain twenty one (21) entries. After the optimized path compression process has been applied there are only five (5) tables that contain eleven (11) entries. The memory space saving is almost forty eight percent (48%).

[0085] In addition, the number of memory accesses needed to traverse the table is also significantly reduced. In the original structure in order to search prefix P0 it is necessary to perform four (4) memory accesses in four (4) pipeline stages.

> With the table in pipeline stage two (2) removed, the number of memory accesses required to traverse the new data structure is reduced to three (3) memory accesses.
> [0086] Similarly, the necessity for memory accesses in pipeline stages two (2), three (3), four (4), and six (6) has been eliminated for searches on prefixes P1 through P5.

As described, Applicants are unable to find any teaching or suggestion that the skip count of Huang refers to consecutive **identical** symbols.

By contrast, a consecutive symbols table of the Applicants' disclosure relates to consecutive identical symbols. Paragraphs [0062] to [0066] of the present disclosure, for example, state:

> [0062] According to an exemplary embodiment of the present invention, at least one consecutive symbols table may be associated with each stage of trie tree lookup tables 260. By way of example, a first **Consecutive 0 Symbols** table may be associated with the first stage of IPv6 trie tree lookup tables 262. The first **Consecutive 0 Symbols** table is searched whenever a string of consecutive 4-bit symbols equal to **0000** is detected that begins with the 4-bit symbol used to search the first stage of IPv6 trie tree lookup tables 262.
> ...
> [0066] Accordingly, similar Consecutive 0 Symbols tables may be associated with each stage in IPv6 trie tree lookup tables 262 and with each stage in IPv4 trie tree lookup tables 261. However, it may desirable to detect consecutive symbols other than **consecutive 0 symbols**. Thus, each stage of IPv6 trie tree lookup tables 262 and each stage of IPv4 trie tree lookup tables 261 may be associated with **tables of consecutive 1 symbols, consecutive 2 symbols, consecutive 3 symbols, and so forth**. (Emphasis added by Applicants.)

Paragraphs [0081] to [0085] of the Applicants' disclosure further state:

> [0081] ... Counts of runs of **identical** symbols are made and only the symbol value and count are needed for the lookup. Microengine 401 compares the 4-bits symbols (S) and makes the following determinations:
> [0082] 1) The symbol S_i for Trie Tree Stage (i) does not equal the symbol S_{i-1} for the previous Trie Tree Stage (i-1). Alternatively, microengine 401 determines that the received AP is from CAM 250 and that this is Trie Tree Stage 1 (i.e., no

previous trie tree stage).

[0083] 2) The symbol S_i for Trie Tree Stage (i) does not equal the symbol S_{i+1} for the next Trie Tree Stage (i+1).

[0084] 3) Since symbol S_i for Trie Tree Stage (i) is not the start of a consecutive symbol string, consecutive symbols tables 264 will be ignored and IPv6 trie tree lookup tables 262 will be searched.

[0085] 4) Symbols S_{i+1}, S_{i+2}, S_{i+3}, and S_{i+4} are the same. Symbol Si_{+5} is different. Thus, a string of four consecutive **identical** symbols (n=4) has been encountered, starting with symbol S_{i+1} and Trie Tree Stage (i+1).

The Applicants have amended the claims to further emphasize that counts of runs of **identical** symbols are made. Accordingly, Applicants respectfully submit that Claim 1 is patentable over the cited references and respectfully request the Examiner to withdraw the § 103 rejection with respect to Claim 1.

Independent Claims 11 and 21 have been amended to recite limitations analogous to the novel limitations emphasized above in traversing the rejection of Claim 1 and, therefore, also are patentable over the cited references. Additionally, Claims 2-10, 12-20, and 22-24 depend from Claims 1, 11, and 21 respectively, and include all the limitations of their respective base claims. As such, Claims 2-10, 12-20, and 22-24 also are patentable over the cited references.

Accordingly, the Applicants respectfully request the Examiner to withdraw the § 103 rejections with respect to Claims 2-24.

ALLOWABLE SUBJECT MATTER

The Examiner objected to Claims 6-10 and 16-20 as being dependent upon a rejected base claim, but suggested that Claims 6-10 and 16-20 would be allowable if it were rewritten in

independent form including all the limitations of the base and intervening claims. The Applicants thank the Examiner for this suggestion but elect not to rewrite Claims 6-10 and 16-20 at this time.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@munckcarter.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP

John T. Mockler

Date: April 2, 2009

John T. Mockler
Registration No. 39,775

P.O. Drawer 800889
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *jmockler@munckcarter.com*